

REMARKS/ARGUMENTS

Claims 1-18, 42, 45, 47 and 53 are pending in the application. Applicant would like to thank the Examiner for indicating that claims 42, 45 and 47 are allowed and that claims 3-18 are allowable.

Claims 1 and 2 are rejected as anticipated by ASANO Japanese Patent Abstract 10-107042.

Reconsideration and withdrawal of the rejection are respectfully requested as the reference does not disclose or suggest a hetero-junction bipolar transistor having at least one electrode contact layer which contacts directly with at least one of collector, base and emitter electrodes as recited in claim 1 of the present application.

By way of example, Figure 1 of the present application shows a hetero-junction bipolar transistor 100 having an electrode contact layer 18 that directly contacts with at least base electrode 21.

The Official Action offers element 20 of ASANO as an electrode contact layer and element 22 as an electrode. As seen in Figure 1 of ASANO, collector layers 13 and 14 are between etch stop layer 20 (electrode contact layer) and element 22 (electrode). Accordingly, ASANO does not disclose or suggest at least one electrode contact layer which contacts directly with at

least one of collector, base and emitter electrodes as recited in claim 1 of the present application.

Claim 2 depends from claim 1 and further defines the invention and is also believed patentable over ASANO.

Claim 53 is rejected as unpatentable over ASANO in view of PRASAD et al. 5,268,315. This rejection is respectfully traversed.

PRASAD et al. is cited for the teaching of a plurality of first level interconnects and a plurality of co-planar second level interconnects. PRASAD et al. does not teach or suggest a hetero-junction bipolar transistor having at least one electrode contact layer that directly contacts with at least one of collector, base and emitter electrodes. As set forth above regarding claim 1, ASANO does not teach this feature. Accordingly, the above-noted feature is missing from each of the references, is absent from the combination and thus is not obvious to one having ordinary skill in the art.

In addition, PRASAD et al. does not teach that for which it is offered. Specifically, elements 66, 54 and 40 are indicated in PRASAD et al. as the collector, base and emitter, respectively. As seen in Figure 15 of PRASAD et al., a contact layer is between each of first level interconnects 86 and the collector, base and emitter 66, 54 and 40. Accordingly, PRASAD et al. does not teach a plurality of first level interconnects

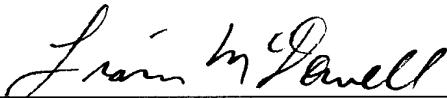
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directly contacting each of the collector, base and emitter electrodes. Further, as seen in Figure 15, the second layer interconnects 100, 102 are not coplanar. Specifically, column 7, lines 40-50 of PRASAD et al. teach that the basic structure is a truncated pyramidal shape having a ramped sidewall profile. Each of the levels of the pyramid are different for layers 100 and 102 and are not coplanar.

In view of the foregoing remarks, it is believed that the present application is in condition for allowance. Reconsideration and allowance are respectfully requested.

Respectfully submitted,

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